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ADS

HW2: VGA and Fixed-Point Arithmetic

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1. VGA color signals are analog, but the outputs of the FPGA are digital. As shown in Section 3.8 of the DE10-Lite manual, each analog color line is driven by four digital pins using a resistor ladder. How many colors can the board output through the VGA interface?

Where n is the DAC resolution and each color is 4-bit.

1. If we aim to drive our VGA output at a 640 × 480 resolution at a 60 Hz refresh rate, what should the pixel clock rate be?

For VGA to output 640 x 480 at 60Hz, the pixel clock rate would been to be 25MHz.

1. In the diagram below, identify and label the following: horizontal front porch, horizontal back porch, horizontal sync pulse, vertical front porch, vertical back porch, vertical sync pulse. Please note that the diagram is not to scale!

A graph of different colored lines

Description automatically generated

Black: Horizontal Back Porch (rising edge)

Purple: Horizontal Front Porch (falling edge)

Gold: Vertical Back Porch (rising edge)

Brown: Vertical Front Porch (falling edge)

Horizontal Pulse: the low signal on the hsynce line

Vertical Pulse: the low signal on the vsynce line

These results are based off Figure 3-22 in the Max10 manual.

A diagram of a device

Description automatically generated

1. For a 640 × 480 resolution at a 60 Hz rate, provide the timings for the following measures in the given units. What is the polarity of the sync pulses on 640x480?

|  |  |  |
| --- | --- | --- |
| Horizontal Front Porch | 16 | Pixels |
| Horizontal sync pulse width | 96 | Pixels |
| Horizontal Back Porch | 48 | Pixels |
| Vertical Front Porch | 10 | Lines |
| Vertical sync pulse width | 2 | Lines |
| Vertical Back Porch | 33 | Lines |

The polarity of the sync pulses are negative.

1. Given the timings in Question 4 and the clock rate in Question 2, what percentage of the frame is spent in the blanking periods?
2. [Bonus] Video output can be done using what is commonly termed as buffering. We utilize a memory or an area of memory called the framebuffer where we store the image data to be shown. Once it has been drawn, we allow our video output to send the image to a display device. While this image is being rendered on the display device, we can prepare a different image to be shown in a different memory or area of memory. Once the display device enters the vertical blanking period, we switch memories or area of memory allowing the newly prepared image to be sent to the display device. While this new image is rendered, we can prepare another image in the memory or memory area that was initially used. As such, drawing an image and displaying the image occurs in parallel without showing artifacts on the display device as long as we keep alternating the memory being written to and the memory being read from (or memory area). This technique is called double buffering. If we allow a 4 bit framebuffer, that is a framebuffer where every pixel only has a 4 bit color value, on a 640 × 480 resolution. How much memory do we need to hold this data? Can we do double buffering at this resolution using only the on-chip memory of the MAX 10 FPGA on the DE10-Lite board?

4-bit frame buffer

Every pixel has a 4-bit color value

640x480 resolution

We would need 154 kilobytes of memory to create a 4-bit framebuffer. Therefore, we would need around 308 KB of memory to do double frame buffering. The DE10-Lite board has 64MB of memory so, we can perform double frame buffering with the Max 10 FPGA.

1. [Bonus] In the next two projects, we will work using a VGA output. The second project will require the use of a 1920×1080 resolution driven at 60 Hz. Provide the timing data for this resolution. What is the sync polarity?

<https://projectf.io/posts/video-timings-vga-720p-1080p/>

Pixel Clock 148.5 MHz

TMDS Clock 1,485.0 MHz

Pixel Time 6.7 ns ±0.5%

Horizontal Freq. 67.500 kHz

Line Time 14.8 μs

Vertical Freq. 60.000 Hz

Frame Time 16.7 ms

Horizontal Timings

Active Pixels 1920

Front Porch 88

Sync Width 44

Back Porch 148

Blanking Total 280

Total Pixels 2200

Sync Polarity pos